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(71) Applicant: **CONEXANT SYSTEMS, INC.** [US/US]; 4311 Jamboree Road, Newport Beach, CA 92660-3095 (US).

(72) Inventors: **SHERMAN, Phil, N.**; 4 Blue Ridge, Irvine, CA 92620 (US). **ZHANG, Zhe**; 170 Giotto, Irvine, CA 92614 (US).

(74) Agent: **FARJAMI & FARJAMI, LLP**; 16148 Sand Canyon, Irvine, CA 92618 (US).

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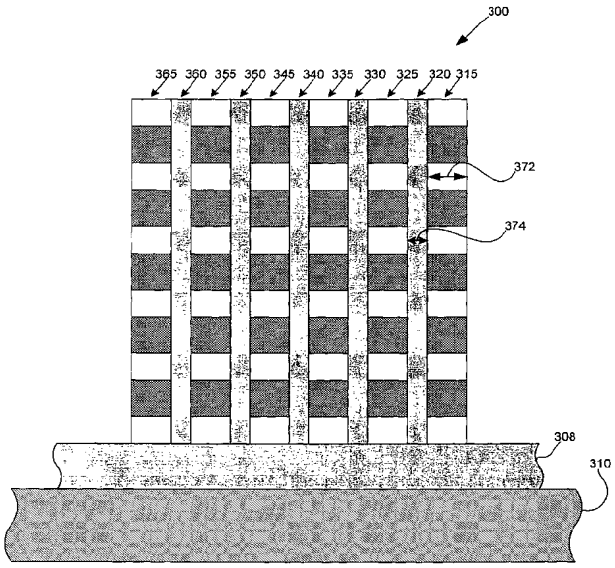

(57) Abstract: A capacitor (300) comprising a plurality of dielectric plates (320, 330, 340, 350, 360) fabricated between every two metal plates from a plurality of metal plates (315, 325, 335, 345, 355, 365) is disclosed. Each metal plate comprises alternating interconnect metal segments and via metal segments. A first group of metal plates are electrically interconnected to form a first electrode of the capacitor. A second group of metal plates are also electrically interconnected to form a second electrode of the capacitor. The interconnect metal segments in each metal plate are typically made of copper or aluminum while the via metal segments in each metal plate are typically made of copper or tungsten. The dielectric plates are typically made of silicon dioxide.

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AN IMPROVED CAPACITOR IN SEMICONDUCTOR CHIPS

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention is generally in the field of semiconductor chips. In particular the present invention is in the field of capacitors used in semiconductor chips.

2. BACKGROUND ART

Figure 1 shows a cross section of a conventional parallel plate capacitor 100. A dielectric layer 104 is shown as sandwiched between top plate 102 and bottom plate 106. Top plate 102 is typically made of conductive material such as titanium nitride while bottom plate 106 is typically made of a different conductive material such as aluminum/copper. Bottom plate 106 might rest on a dielectric layer such as inter-layer dielectric ("ILD") 108 which in turn rests on a metal layer or a semiconductor substrate. By way of example, Figure 1 shows that ILD 108 rests on semiconductor substrate 110.

It is well known that the capacitance value of a parallel plate capacitor, such as parallel plate capacitor 100, is calculated by the equation:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{t} \qquad \text{(Equation 1)}$$

where ε_0 is the permittivity of the free space ($\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm), ε_r is the relative permittivity (also referred to as dielectric constant or "k"), A is the surface area of plate 102 (or plate 106) and t is the thickness of dielectric layer 104.

Given the capacitance Equation 1, device engineers can increase capacitance by either decreasing the dielectric thickness t, using material with a high dielectric constant ε_r, or increasing the surface area A. However, device engineers have to work with the physical design limitations and electrical requirements in the circuit when adjusting the variables in capacitance Equation 1 in their attempt to increase capacitance.

Device engineers need a way to increase the capacitance without taking up the limited device surface area. As shown in Figure 1, in parallel plate capacitor 100, plates 102 and 106 are laid out in parallel to the surface of semiconductor substrate 110. The size of parallel plates 102 and 106 can be increased in order to increase the capacitance of parallel plate capacitor 100. However, it is undesirable to consume the already limited surface area of a semiconductor die for building large capacitors.

In fact, as geometries of active circuits in semiconductor dies decrease, it becomes less and less desirable to allocate large portions of semiconductor die surface area for building parallel plate capacitors such as capacitor 100. Thus, a major problem with prior art parallel plate capacitor 100 is the amount of surface area that the two plates 102 and 106 occupy. In addition to the undesirable waste of semiconductor die surface area, increasing the size of parallel plates 102 and 106 cause other

problems. For example, when a conventional chemical mechanical polishing ("CMP") is used to planarize the surface of metal, a well-known "dishing" problem occurs in wide metal features, such as plates 102 and 106 in capacitor 100.

Referring to Equation 1, since capacitance C is inversely proportional to the dielectric thickness *t*, another way to increase the capacitance is by decreasing the thickness of dielectric layer 104. However, process limitations such as an unacceptable increase in defect density of thin dielectrics prevent use of very thin dielectrics. Also, as dielectric layer 104 becomes thinner, capacitance of capacitor 100 increasingly becomes a function of the voltage across parallel plates 102 and 104. By decreasing the thickness of dielectric layer 104, parallel plate capacitor 100 manifests additional problems such as a low break down voltage and a high leakage current. A combination of all of these problems prevents use of very thin dielectrics in parallel plate capacitors such as capacitor 100.

Further, in a number of semiconductor applications, accurate "matching" of capacitors is necessary. Capacitors are matched if their absolute values can be determined and replicated with accuracy and also if their capacitance values do not vary as a function of external circuit conditions, such as the voltage applied to the capacitor plates. With parallel plate capacitor 100, matching of capacitors is difficult since small variations in the thickness of thin dielectric 104 results in relatively large variations in the capacitance value. Moreover, due to the fact that dielectric 104 is thin and also due to the fact that top plate 102 is made of conductive material different from the conductive material of bottom plate 106, capacitor 100 is a relatively strong function of the voltage applied to the capacitor plates.

Another disadvantage with present parallel plate capacitors such as capacitor 100 is that an extra mask and additional process steps are required so that top plate 102 can be fabricated at a certain desired height (for example, 600 to 800 Angstroms) relative to bottom plate 106. The extra mask and its associated extra processing steps increase fabrication costs of prior art parallel plate capacitor 100.

A further disadvantage of present parallel plate capacitors such as capacitor 100 is that due to the fact that top plate 102 is typically made of material such as titanium nitride which has a relatively low conductivity, the quality factor of capacitor 100 is relatively low. A relatively low quality factor means that there is a relatively high energy loss in the capacitor, which is of course undesirable.

Thus, there is serious need in the art for a capacitor in semiconductor chips that has a high capacitance density, a low defect density, is not a strong function of the voltage applied to the capacitor, has good matching characteristics, has a high break down voltage, can be fabricated at reduced cost, and has a high quality factor.

SUMMARY OF THE INVENTION

The present invention is an improved capacitor in semiconductor chips. The invention's capacitor overcomes the present need for a capacitor which has a high capacitance density, a low defect density, is not a strong function of the voltage applied to the capacitor, has good matching characteristics, has a high break down voltage, can be fabricated at reduced cost, and has a high quality factor.

In one embodiment, the invention is a capacitor having first and second metal plates and a dielectric plate situated between the first and second metal plates. At least one of the metal plates comprises alternating interconnect metal segments and via metal segments. The first and second metal plates form the capacitor electrodes.

In another embodiment, the invention comprises a large number of metal plates and dielectric plates fabricated in an alternating configuration. In other words, there is a dielectric plate between every two metal plates. Each metal plate comprises alternating interconnect metal segments and via metal segments. A first group of metal plates are electrically interconnected to form a first electrode of the invention's capacitor. A second group of metal plates are also electrically interconnected to form a second electrode of the invention's capacitor.

The interconnect metal segments in each metal plate are typically made of copper or aluminum while the via metal segments in each metal plate are typically made of copper or tungsten. The dielectric plates can be made of silicon dioxide or other inter-layer dielectric ("ILD").

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a prior art parallel plate capacitor used in semiconductor chips.

Figure 2 illustrates a cross-section of one embodiment of the invention's capacitor having two metal plates and a dielectric plate situated between the two metal plates.

Figure 3 illustrates a cross-section of another embodiment of the invention's capacitor having six metal plates and a dielectric plate situated between every two metal plates.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is an improved capacitor in semiconductor chips. The following description contains specific information pertaining to different types of materials, layouts, dimensions, and implementations of the invention's capacitor. One skilled in the art will recognize that the present invention may be practiced with material, layout, or dimensions different from those specifically discussed in the present application. Moreover, some of the specific details of the invention are not discussed in order to not obscure the invention. The specific details not described in the present application are within the knowledge of a person of ordinary skill in the art.

The drawings in the present application and their accompanying detailed description are directed to merely example embodiments of the invention. To maintain brevity, other embodiments of the invention which use the principles of the present invention are not specifically described in the present application and are not specifically illustrated by the present drawings.

Figure 2 illustrates a cross section of an embodiment of capacitor 200 of the present invention. As shown in Figure 2, capacitor 200 rests on inter-layer dielectric ("ILD") 208 which in turn rests on a semiconductor substrate 210 in a semiconductor die (the semiconductor die is not shown in any of the Figures). Although it is not the case in the embodiment of the invention shown in Figure 2, capacitor 200 may rest on a particular metal layer instead of resting on inter-layer dielectric 208 shown in Figure 2. Semiconductor substrate 210 is typically made of silicon while dielectric layer 208 is typically made of silicon dioxide. Figure 2 shows respective cross-sections of two metal plates which are marked by numerals 220 and 240. These two cross-sectional views of the metal plates are referred to as plates 220 and 240 for brevity, although they are only cross-sectional views of their respective plates. Metal plates 220 and 240 are parallel to each other and are fabricated perpendicular to dielectric layer 208 and semiconductor substrate 210. Dielectric plate 230 is situated between metal plates 220 and 240. Although Figure 2 shows merely a cross-sectional view of dielectric plate 230, to maintain brevity, that cross-sectional view is referred to as dielectric plate 230.

Metal plate 220 is comprised of segments 212, 214, 216, 218, 220, 222, 224, 226, 228, 232, and 234 stacked on one another as shown in capacitor 200 of Figure 2. Similarly, metal plate 240 is comprised of segments 213, 215, 217, 219, 221, 223, 225, 227, 229, 231, and 233 stacked on one another. Segment 234 in metal plate 220 is made of interconnect metal layer one and forms the base of metal plate 220. Segment 228 is made of interconnect metal layer two and is connected to segment 234 through segment 232. Segment 232 is made from via metal and connects interconnect metal layer one segment 234 with interconnect metal layer two segment 228.

Segment 224 is made of interconnect metal layer three and is connected to segment 228 through segment 226. Segment 226 is made from via metal and connects interconnect metal layer two segment 228 with interconnect metal layer three segment 224. Segment 220 is made of interconnect metal layer four and is connected to segment 224 through segment 222. Segment 222 is made from via

metal and connects interconnect metal layer three segment 224 with interconnect metal layer four segment 220. Segment 216 is made of interconnect metal layer five and is connected to segment 220 through segment 218. Segment 218 is made from via metal and connects interconnect metal layer four segment 220 with interconnect metal layer five segment 216.

Finally, segment 212 is made of interconnect metal layer six and is connected to segment 216 through segment 214. Segment 214 is made from via metal and connects interconnect metal layer five segment 216 with interconnect metal layer six segment 212. Metal layer six segment 212 is the final segment in metal plate 220 and completes the construction of metal plate 220.

In the embodiment of the invention shown in Figure 2, metal plate 240 is configured in exactly the same fashion as metal plate 220, as described above. In particular, segment 233 in metal plate 240 is made of interconnect metal layer one and forms the base of metal plate 240. Segment 229 is made of interconnect metal layer two and is connected to segment 233 through segment 231. Segment 231 is made from via metal and connects interconnect metal layer one segment 233 with interconnect metal layer two segment 229.

Segment 225 is made of interconnect metal layer three and is connected to segment 229 through segment 227. Segment 227 is made from via metal and connects interconnect metal layer two segment 229 with interconnect metal layer three segment 225. Segment 221 is made of interconnect metal layer four and is connected to segment 225 through segment 223. Segment 223 is made from via metal and connects interconnect metal layer three segment 225 with interconnect metal layer four segment 221. Segment 217 is made of interconnect metal layer five and is connected to segment 221 through segment 219. Segment 219 is made from via metal and connects interconnect metal layer four segment 221 with interconnect metal layer five segment 217.

Finally, segment 213 is made of interconnect metal layer six and is connected to segment 217 through segment 215. Segment 215 is made from via metal and connects interconnect metal layer five segment 217 with interconnect metal layer six segment 213. Metal layer six segment 213 is the final segment in metal plate 240 and completes the construction of metal plate 240. As mentioned above, situated between metal plate 220 and metal plate 240 is dielectric plate 230. The combination of metal plate 220 and metal plate 240 and dielectric 230 situated therebetween forms the invention's capacitor. In the present application, metal plates 220 and 240 are also referred to as first and second electrodes of the invention's capacitor.

In the embodiment of the invention shown in Figure 2, interconnect metal layer one segments 234 and 233 are made of copper. However, another metal such as aluminum/copper could be used instead of copper. Similarly, interconnect metal layer two segments 228 and 229, interconnect metal layer three segments 224 and 225, interconnect metal layer four segments 220 and 221, interconnect metal layer five segments 216 and 217, and interconnect metal layer six segments 212 and 213 are all made of copper, although they could be made of another metal such aluminum.

Via metal segments 232 and 231 are also made of copper; however, they could be made of tungsten. Similarly, via metal segments 226 and 227, via metal segments 222 and 223, via metal segments 218 and 219, and via metal segments 214 and 215 are all made of copper, although they could be made of another metal such as tungsten.

When copper is selected as the interconnect metal in a semiconductor fabrication process, interconnect metal segments 234, 228, 224, 220, 216, and 212 in plate 220 and interconnect metal segments 233, 229, 225, 221, 217, and 213 in plate 240 are typically fabricated using a damascene process. In a damascene process, for each interconnect metal layer, the interconnect metal is laid into trenches formed in a dielectric layer. After the metal is laid into dielectric trenches, the metal and dielectric undergo a chemical mechanical polish (CMP) process. The CMP process planarizes the surface of the dielectric and the in-laid interconnect metal and makes the in-laid interconnect metal substantially flush with the surface of the dielectric.

In a typical damascene process when copper is used as the interconnect metal, tungsten is used as via metal. It is also possible to use copper as both the via metal and the interconnect metal. When copper is used as both the via metal and interconnect metal, the process of choice may be a dual damascene process. In a dual damascene process, in addition to etching trenches into a dielectric to lay in interconnect metal, via holes are etched into a dielectric layer above the interconnect metal layer in order to lay copper into the via holes to make electrical connection to the underlying interconnect metal layer. Thus, when copper is used as the via metal in segments 232, 226, 222, 218, and 214 in metal plate 220 and in segments 231, 227, 223, 219, and 215 in metal plate 240, a dual damascene process can be used to fabricate the via segments and also to fabricate the interconnect metal segments.

Figure 2 illustrated a simplified embodiment of the present invention where only two metal plates 220 and 240 were used as first and second electrodes to form the invention's capacitor. However, in practice a large number (typically 25 or more) of metal plates (such as metal plates 220 and 240 in Figure 2) are used to achieve the desired total capacitance and capacitance density. Although in practice 25 or more metal plates are used, Figure 3 serves as a tool to explain the configuration of the invention's capacitor when more than the two metal plates are used. In the embodiment of the invention whose cross-section is shown in Figure 3, the invention's capacitor 300 comprises six metal plates 315, 325, 335, 345, 355, and 365. Separating the metal plates are dielectric plates 320, 330, 340, 350, and 360. Metal plates 315, 325, 335, 345, 355, and 365 and dielectric plates 320, 330, 340, 350, and 360 rests on inter-layer dielectric ("ILD") 308 which is in turn fabricated on semiconductor substrate 310. Although it is not the case in the embodiment of the invention shown in Figure 3, capacitor 300 may rest on a particular metal layer instead of resting on inter-layer dielectric 308 shown in Figure 3.

In one embodiment of the invention, semiconductor substrate 310 is made of silicon while dielectric layer 308 is made of silicon dioxide. In that embodiment of the invention, each dielectric

plate 320, 330, 340, 350, and 360 can also be made of silicon dioxide. In the same manner that was illustrated and described with respect to metal plates 220 and 240 in Figure 2, each metal plate 315, 325, 335, 345, 355, and 365 in Figure 3 consists of alternating interconnect metal segments and via metal segments. In one embodiment of the invention, the interconnect metal segments are made of copper while the via metal segments are made of tungsten. In another embodiment of the invention, both interconnect metal segments and via metal segments are made of copper. In the embodiment of the invention shown in Figure 3, width 372 of each metal plate can be approximately 0.50 microns, depending on the technology, and width 374 of each dielectric plate can be approximately 0.23 microns, but this width can vary depending on the lithography technology, break down voltage, leakage current, and other factors affecting the acceptable dimension for width 374.

Although not shown in Figure 3, metal plates 315, 335, and 355 are electrically interconnected to each other and form a first capacitor electrode. Likewise, metal plates 325, 345, and 365 are also electrically interconnected to each other and form a second capacitor electrode. Metal plates 315, 335, and 355 are electrically connected to each other through an interconnect pattern using interconnect metal layer six which is the topmost interconnect metal layer in the embodiment of the invention shown in Figure 3. The interconnect pattern connecting metal plates 315, 335, and 355 is not shown in Figure 3. Similarly, metal plates 325, 345, and 365 are connected to each other through an interconnect pattern using the topmost interconnect metal layer which is interconnect metal layer six in the embodiment of the invention shown in Figure 3. The interconnect pattern connecting metal plates 325, 345, and 365 is not shown in Figure 3.

In a typical semiconductor chip, a typical small capacitor is required to be at least 500 fF. In prior art parallel plate capacitor 100 shown in Figure 1, the capacitance density is about 1.0 fF per square micron. Thus, to achieve a capacitance of 500 fF bottom plate 106 must be at least 500 square microns. To achieve an area of 500 square microns, typically top plate 102 and bottom plate 106 are shaped as a square with a side of approximately 22.5 microns (alternatively, top plate 102 and bottom plate 106 can be shaped as rectangles with appropriate dimensions). The capacitance density of about 1.0 fF per square micron in prior art parallel plate capacitor 100 of Figure 1 is achieved using a "high-k" dielectric such as silicon nitride with a thickness of approximately 600 to 800 Angstroms. Due to the small thickness of the dielectric, small variations in the thickness of the dielectric cause relatively large variations in the total capacitance.

Further, due to the small thickness of dielectric 104, top plate 102 must be approximately 600 to 800 Angstroms high relative to bottom plate 106. However, the typical distance between a lower and an upper interconnect metal layer is at least 5000 Angstroms. Thus, while bottom plate 106 is typically made of an interconnect metal layer, top plate 102 is not made of the available overlying interconnect metal layer. Instead, top plate 102 is made from an additional metal layer and patterned by using an additional mask used solely for fabrication of top plate 102 of parallel plate capacitor 100.

In other words, an additional mask is employed so that a conductive material can be fabricated at a specific height determined by factors such as the minimum required break down voltage and maximum permissible leakage current. As an example, the specific height of top plate 102 relative to bottom plate 106 can be approximately 600 to 800 Angstroms. An example of a conductive material which may be used as top plate 102 and fabricated by the additional mask is titanium nitride. The additional mask and its associated additional processing steps increase fabrication costs of prior art parallel plate capacitor 100.

Linear and quadratic voltage coefficients are used to model the change in capacitance value of a capacitor as a function of voltage difference between the capacitor plates. For that purpose, linear and quadratic voltage coefficients are used in the well known equation $C = C_0 (1 + aV + bV^2)$ (Equation (2)). In Equation (2) coefficient "a" is the linear voltage coefficient, coefficient "b" is the quadratic voltage coefficient, and variable "V" is the voltage difference between the capacitor plates (variable "V" is also referred to as the voltage across the capacitor plates or the voltage applied to the capacitor). Constant C_0 is the capacitance value when no voltage is applied to the capacitor plates, i.e. when "V" is equal to zero. And "C" is the actual capacitance value when voltage "V" is applied to the capacitor plates.

Ideally, the capacitance value should be independent of the voltage across the parallel plates of a capacitor. However, in case of prior art parallel plate capacitor 100 described above, the linear voltage coefficient "a" and the quadratic voltage coefficient "b" in Equation (2) are relatively high. Because of the fact that the values of coefficients "a" and "b" in Equation (2) are relatively high, prior art capacitor 100 is a relatively strong function of the voltage across top plate 102 and bottom plate 106. This, of course, is an undesirable characteristic of prior art parallel plate capacitor 100.

One reason that prior art capacitor 100 is a relatively strong function of the voltage across the parallel plates is that top plate 102 is made of conductive material different from conductive material of bottom plate 106. Typically, bottom plate 106 is made of aluminum/copper with a thickness of approximately 5000 Angstroms. Sheet resistivity of aluminum at a thickness of 5000 Angstroms is about 0.08 ohms per square. However, top plate 102 is typically made of titanium nitride with a thickness of approximately 2000 Angstroms. Sheet resistivity of titanium nitride at a thickness of 2000 Angstroms is about 16.0 ohms per square. Thus, top plate 102 has a significantly lower conductivity than bottom plate 106. This difference in conductivities of the top and bottom plates of the capacitor contributes to capacitor 100 being a relatively strong function of the voltage across top plate 102 and bottom plate 106.

Another reason that prior art capacitor 100 is a relatively strong function of the voltage across parallel plates 102 and 106 is the small thickness of dielectric 104. It is known in the art that a thin capacitor dielectric, for example a dielectric having a thickness of approximately 600 to 800 Angstroms, contributes to the "non-linearity" of prior art parallel plate capacitor 100.

The relatively high resistance of top plate 102 in capacitor 100 also results in a lower "quality factor" for prior art capacitance 100. Quality factor is inversely proportional to energy loss in a capacitor and as such a low quality factor is undesirable. One of the factors that results in a low quality factor of a capacitor is the resistance in series with one (or both) of the capacitor plates. A high series resistance results in a high energy loss and a low quality factor. Since prior art parallel plate capacitor 100 described above typically employs a top plate made of titanium nitride (as opposed to the more conductive aluminum or copper) the series resistance in top plate 102 is relatively high. The series resistance of top plate 102 is high also because top plate 102 is typically only 2000 Angstroms thick (as opposed to the thickness of, for example, bottom plate 106 which is 5000 Angstroms). As stated above, sheet resistivity of titanium nitride at a thickness of 2000 Angstroms is about 16.0 ohms per square.

In contrast to the prior art parallel plate capacitor 100, the invention's capacitor provides a high capacitance density, a low defect density, a capacitance value that is less dependent on the voltage across the capacitor metal plates, good matching characteristics, and a high quality factor. Moreover, the invention provides these advantages without requiring any additional mask or processing step.

In contrast to prior art parallel plate capacitor 100 shown in Figure 1, the invention can easily provide a capacitance density of approximately 1.25 fF per square micron and even more. That is, the invention can provide an increase of at least 25% or more in capacitance density. In a six layer metal process such as that discussed in relation to Figures 2 and 3, the typical width 372 of each metal plate can be approximately 0.50 microns, depending on the technology. Also, the typical width 374 of each dielectric plate occupying the space between two neighboring metal plates can be approximately 0.23 microns, but this width can vary depending on the lithography technology, break down voltage, leakage current, and other factors affecting the acceptable dimension for width 374. With these dimensions, approximately 25 to 30 metal plates such as those shown in Figure 3 are used to make up the total capacitance of 500 fF. The 25 to 30 metal plates occupy an area of approximately 400 square microns, resulting in a capacitance density of 1.25 fF per square micron for the invention's capacitor.

As is well known in the art the number of metal layers fabricated on a semiconductor chip continually increases. The invention's principals can be even more advantageously applied as the number of metal layers increases. Some semiconductor manufacturers already fabricate ten metal layers and others are moving towards that goal. With ten metal layers even when width 372 (Figure 3) of metal plates remains at 0.50 microns and width 374 (Figure 3) of dielectric plates remains at 0.23 microns, the capacitance density achieved by the present invention is approximately 2.50 fF per square micron. This is clearly a significant improvement in the capacitance density of approximately 1.0 fF per square micron achieved by prior art parallel plate capacitor 100 in Figure 1. Moreover, a number of semiconductor manufacturers are already able to reduce dielectric width 374 (Figure 3) from 0.23 microns to approximately 0.10 microns (i.e. 1000 Angstroms). Since capacitance of a capacitor is

inversely proportional to the dielectric thickness, the reduction in dielectric thickness to 0.10 microns will further increase the capacitance density achieved in the present invention.

As discussed above, width 374 of the dielectric plate of the embodiment of the invention's capacitor shown in Figure 3 is 0.23 microns (i.e. 2300 Angstroms). This width (or thickness) of the invention's dielectric plate is much greater than the 600 Angstrom to 800 Angstrom thickness of dielectric 104 in prior art parallel plate capacitor 100. Due to the greater thickness of the dielectric of the invention's capacitor, the defect density of the invention's capacitor is much lower than prior art parallel plate capacitor 100. Even when width (or thickness) 374 of the invention's dielectric plate is reduced to 0.10 microns (i.e. 1000 Angstroms), the invention still has an improved defect density relative to prior art parallel plate capacitor which has a dielectric thickness of merely 600 to 800 Angstroms.

Since width (or thickness) 374 (Figure 3) of the dielectric plate in the invention's capacitor is greater than the thickness of dielectric layer 104 in prior art parallel plate capacitor 100, the invention's capacitor is substantially independent from the voltage across the capacitor's electrodes. Referring to Equation (2) above, coefficients "a" and "b" in the invention's capacitor are substantially equal to zero. In other words, the invention's capacitor shown in Figures 2 and 3 has a substantially constant capacitance which is substantially independent from the voltage "V" (Equation (2)) across the capacitor's electrodes.

It is recalled that the difference in conductivity between the capacitor plates was a contributing factor in making prior art parallel plate capacitor 100 a strong function of voltage. In contrast, such difference in conductivity does not exist between the metal plates of the invention's capacitor. The metal plates of the invention's capacitor are entirely symmetrical in that the constituent interconnect metal segments and via metal segments in each capacitor plate are the same as any other capacitor plate.

For example, when the interconnect metal segments in the invention's capacitor are made of copper and the via metal segments are made of tungsten, all metal plates have the same conductivity since they are all made of the same alternating segments of copper and tungsten. Alternatively, when the interconnect metal segments are made of copper and the via metal segments are also made of copper, all metal plates still have the same conductivity since all metal plates are uniformly made of copper. Moreover, the width (or thickness) and length of all metal plates are exactly the same. Accordingly, the conductivities of all metal plates in the invention's capacitor are the same. The equal conductivities of all metal plates in the invention's capacitor contributes to the fact that the invention's capacitor is substantially independent of the voltage across the capacitor electrodes.

Due to the relatively large thickness of the invention capacitor's dielectric plates, small variations in dielectric thickness do not cause a great change in the total capacitance value. Moreover, as explained above, the invention's capacitor has a substantially constant capacitance value which is

independent of the voltage applied to the capacitor electrodes. Accordingly, the invention's capacitor has good matching characteristics since its capacitance value can be determined and replicated with accuracy.

It is noted that because of the fact that the thickness of the dielectric plate used in the present invention (the thickness being approximately 2300 Angstroms) is much larger than the thickness of the dielectric in the prior art parallel plate capacitor (the thickness being approximately 600 to 800 Angstroms), the break down voltage of the invention's capacitor is substantially higher than the break down voltage of the prior art parallel plate capacitor. Moreover, due to the thicker dielectric of the invention's capacitor, the leakage current in the invention's capacitor is substantially lower than the leakage current in the prior art parallel plate capacitor.

The invention's capacitor also has a higher quality factor than that of the prior art parallel plate capacitor 100 in Figure 1. As discussed in relation to Figure 3, the invention capacitor's metal plates typically have a width (or thickness) of approximately 0.50 microns. At a thickness of 0.50 microns, each interconnect metal segment of the invention's capacitor that is made of copper has a sheet resistivity of only 0.04 ohms per square. Even in the embodiment of the invention using alternating segments of copper and tungsten, the total resistance of each metal plate in the invention is less than the total resistance of the titanium nitride in top plate 102 in prior art capacitor 100. In fact, due to lower resistivity of copper and the fact that the invention's metal plates are only about 10.0 microns long for a ten layer metal process and even shorter (approximately 6.0 microns long) for a six layer metal process, the alternating segments of copper and tungsten in the invention's metal plates result in resistivity that is even lower than the aluminum in bottom plate 106 in prior art capacitor 100. The reason is that aluminum has higher resistivity than copper and also the aluminum bottom plate 106 in prior art capacitor 100 is usually much longer than 10.0 microns.

Another advantage of the invention over prior art parallel plate capacitor 100 is that the width (or thickness) 374 (Figure 3) of each dielectric plate in the invention's capacitor can be substantially less than 0.23 microns. It is recalled that capacitance densities of 1.25 fF per square micron for a six layer metal process and 2.50 fF per square micron for a ten layer metal process were achievable using dielectric plates with a thickness of 0.23 microns. These capacitance densities, i.e. capacitance density of 1.25 fF per square micron for a six layer metal process and capacitance density of 2.50 fF per square micron for a ten layer metal process, can be substantially increased when the dielectric thickness is reduced from 0.23 microns to 0.10 microns. In contrast, the thickness of 600 to 800 Angstroms for prior art dielectric layer 104 described in relation to Figure 1 is already so small such that it is very difficult to improve the capacitance density of prior art parallel plate capacitor 100 without encountering defect densities that are too high to be acceptable. Accordingly, while the invention allows for a substantial increase in capacitance density, prior art parallel plate capacitor 100 does not allow a substantial increase in capacitance density.

It is noted that the although Figures 2 and 3 showed the invention's capacitors 200 and 300 resting on, respectively, inter-layer dielectrics ("ILD") 208 and 308, the invention's capacitors 200 or 300 may rest on a particular metal layer instead of resting on an inter-layer dielectric.

The invention's advantages discussed above are achieved without any requirement for an additional mask or additional processing steps. In fact, since the invention's capacitor is fabricated with standard fabrication processes, the invention results in a reduction of fabrication costs as compared with the costs for fabricating prior art parallel plate capacitor 100. The reason is that prior art capacitor 100 requires an additional mask and additional processing steps for fabrication of top plate 102, while the invention's capacitor does not require any additional masks or processing steps.

From the above description of the invention, it is manifest that various material can be used for metal plates and dielectric plates in the present invention without departing from the scope of the present invention. Moreover, while the invention has been described with specific reference to certain embodiments, materials, and dimensions, a person of ordinary skills in the art would recognize that changes can be made in form and detail without departing from the spirit and the scope of the invention. The described embodiments are to be considered in all respects as illustrative and not restrictive. It should also be understood that the invention is not limited to the particular embodiments described herein, but is capable of many rearrangements, modifications, and substitutions without departing from the scope of the invention.

As explained above, the invention's capacitor has overcome the present need for a capacitor which has a high capacitance density, a low defect density, is not a strong function of the voltage applied to the capacitor, has good matching characteristics, can be fabricated at reduced cost, and has a high quality factor.

Thus, an improved capacitor in semiconductor chips has been described.

CLAIMS

1. A capacitor comprising:

a first metal plate, a second metal plate, and a dielectric plate situated between said first and second metal plates;

said first metal plate comprising a first metal layer one segment, a first via metal segment fabricated on top of and contacting said first metal layer one segment, and a first metal layer two segment fabricated on top of and contacting said first via metal segment.

2. The capacitor of claim 1 wherein said second metal plate comprises a second metal layer one segment, a second via metal segment fabricated on top of and contacting said second metal layer one segment, and a second metal layer two segment fabricated on top of and contacting said second via metal segment.

3. The capacitor of claim 1 wherein said first metal layer one segment is selected from the group consisting of copper and aluminum.

4. The capacitor of claim 1 wherein said first via metal is selected from the group consisting of tungsten and copper.

5. The capacitor of claim 1 wherein said first metal layer two segment is selected from the group consisting of copper and aluminum.

6. The capacitor of claim 2 wherein said second metal layer one segment is selected from the group consisting of copper and aluminum.

7. The capacitor of claim 2 wherein said second via metal is selected from the group consisting of tungsten and copper.

8. The capacitor of claim 2 wherein said second metal layer two segment is selected from the group consisting of copper and aluminum.

9. The capacitor of claim 1 wherein said dielectric plate comprises silicon dioxide.

10. A capacitor comprising:

a plurality of metal plates, each of said plurality of metal plates comprising a plurality of interconnect metal layer segments and a plurality of via metal segments;

a plurality of dielectric plates, each of said plurality of dielectric plates being situated between two of said plurality of metal plates;

a first group of said plurality of metal plates being electrically interconnected to form a first electrode of said capacitor;

a second group of said plurality of metal plates being electrically interconnected to form a second electrode of said capacitor.

11. The capacitor of claim 10 wherein each of said plurality of interconnect metal layer segments comprises copper.

12. The capacitor of claim 10 wherein each of said plurality of interconnect metal layer segments comprises aluminum.

13. The capacitor of claim 10 wherein each of said plurality of via metal segments comprises aluminum.

14. The capacitor of claim 10 wherein each of said plurality of via metal segments comprises tungsten.

15. The capacitor of claim 10 wherein each of said plurality of dielectric plates comprises silicon dioxide.

16. The capacitor of claim 10 wherein each of said plurality of metal plates comprises at least six interconnect metal layer segments.

17. The capacitor of claim 10 wherein each of said plurality of metal plates comprises at least ten interconnect metal layer segments.

18. The capacitor of claim 10 wherein said plurality of metal plates comprises at least twenty five metal plates.

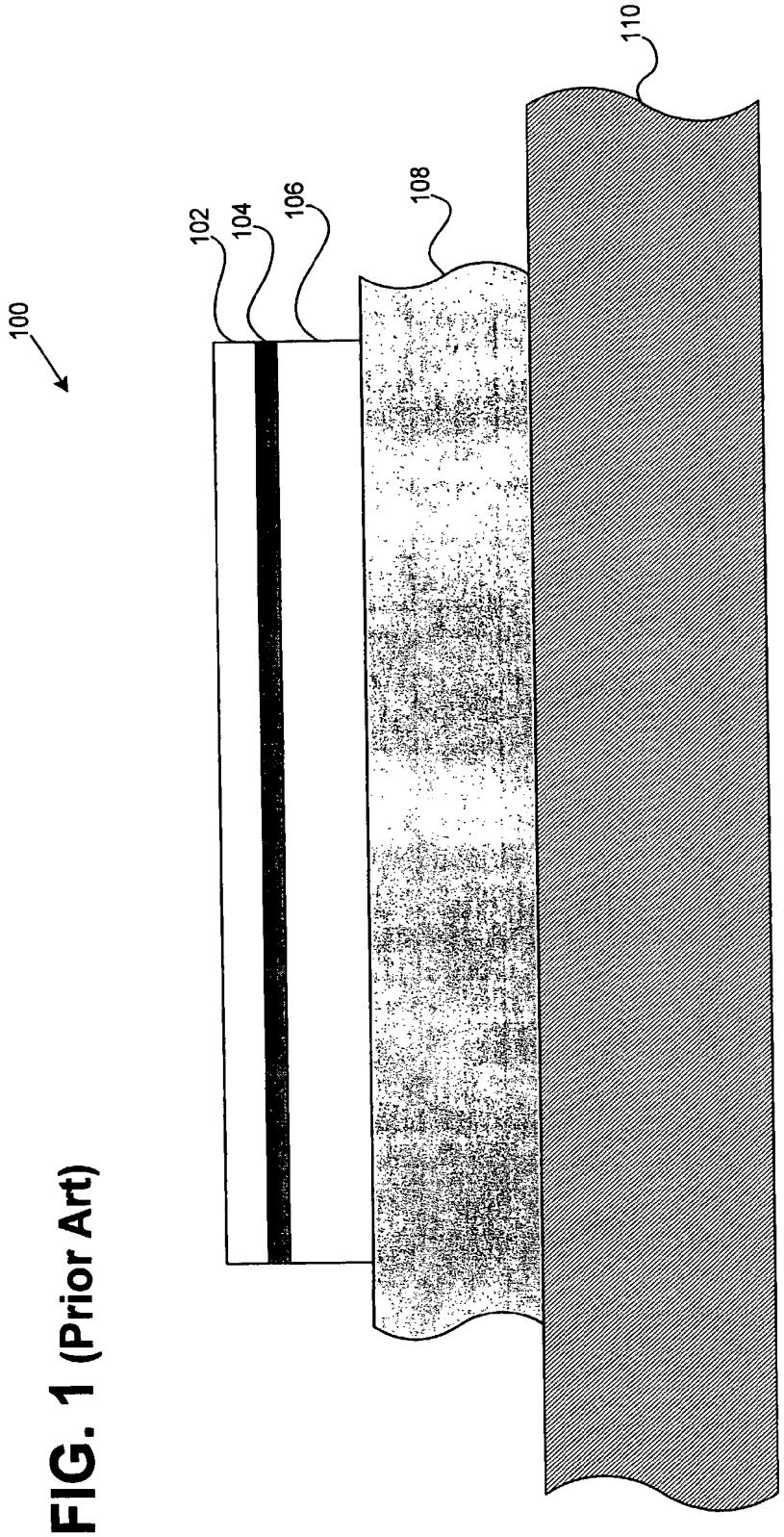

FIG. 1 (Prior Art)

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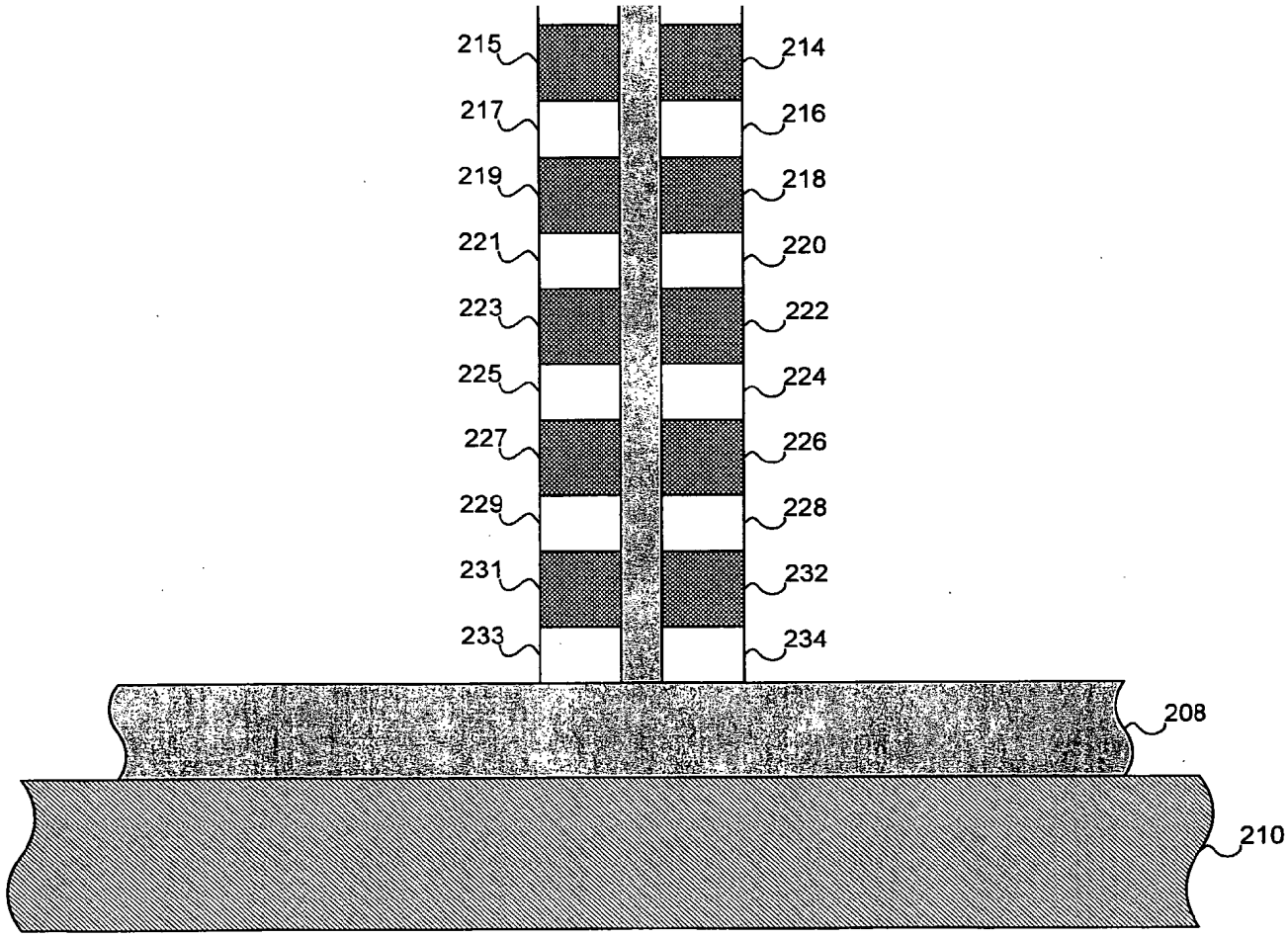
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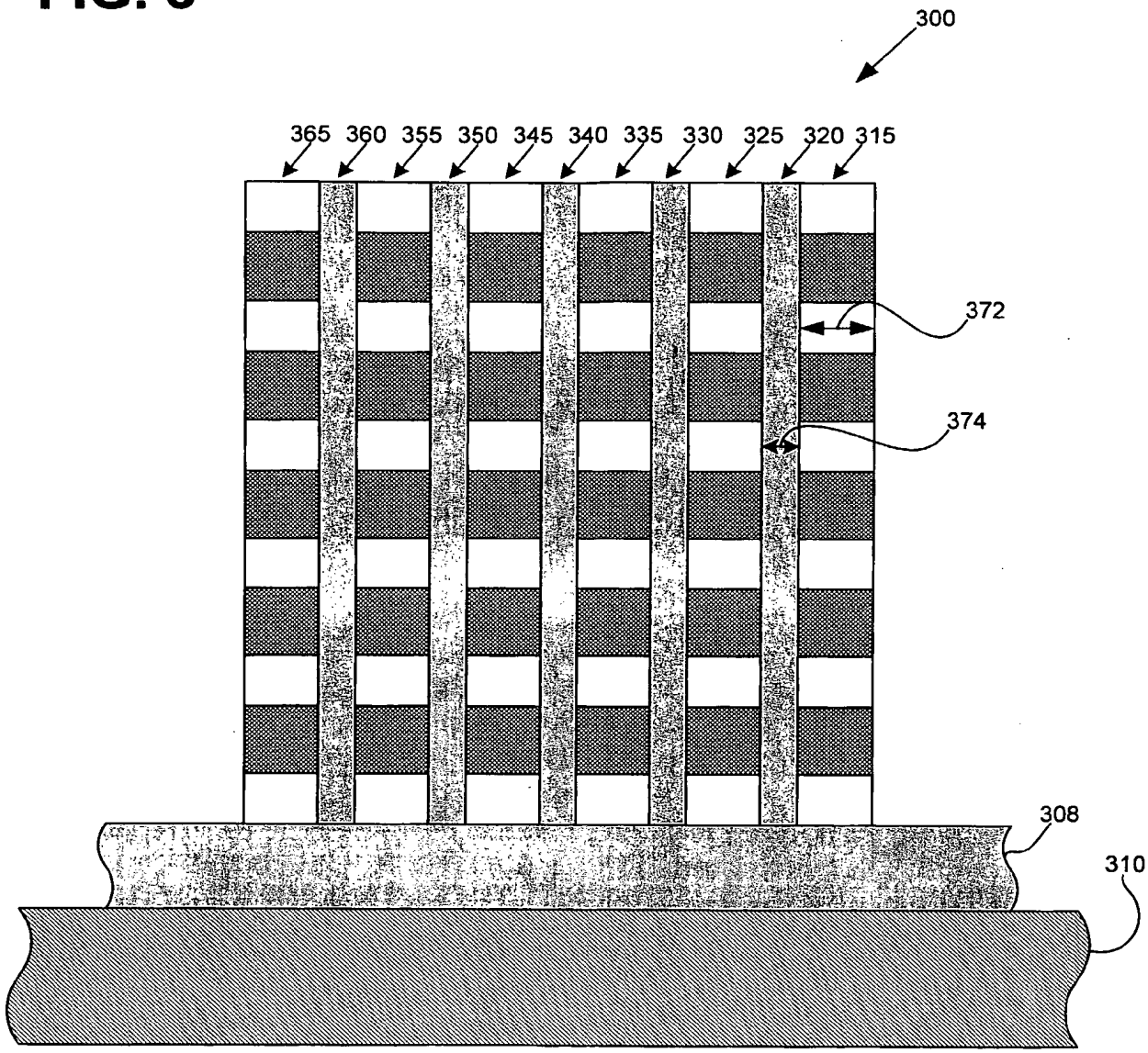
FIG. 3



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/04545

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 29/00
US CL : 257/532
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/68, 71, 295-313, 532, 534,905-908; 438/239,243, 244, 381, 387, FOR430

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
search terms: electrode, plate, copper, capacitor, vertical cell, vertical capacitor, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,583,359 A (Ng et al.) 10 December 1996 (10.12.1996), figure 3, column 1, lines 27-	1-17
---	28, column 3, lines 5-7, column 4, lines 25-32, column 8, lines 58-64, column 14, lines 23-	------
Y	25.	18
Y	US 5,336,630 A (Yun et al.) 09 August 1994 (09.08.1994), abstract, figure 3e, figure 4h, column 1, line 46, column 5, lines 26-30, 37-40	1-18
Y,P	US 6,169,356 B1 (Ohnishi et al.) 02 January 2001 (02.01.2001), column 5, lines 36-44,	1-8, 10-14, 16-17
A	US 4,700,457 A (Matsukawa) 20 October 1987 (20.10.1987)	1-18
A	US 4,929,998 A (Boudewijns) 29 May 1990 (29.05.1990)	1-18
A	US 5,077,225 A (Lee) 31 December 1991 (31.12.1991)	1-18
A	US 5,158,905 A (Ahn) 27 October 1992 (27.10.1992)	1-18
A	US 5,241,201 A (Matsuo et al.) 31 August 1993 (31.08.1993)	1-18
A	US 5,346,846 A (Park et al.) 13 September 1994 (13.09.1994)	1-18

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703)305-3230

Authorized officer
Marcos D. Pizarro-Crespo

Telephone No. (703) 308-0956

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